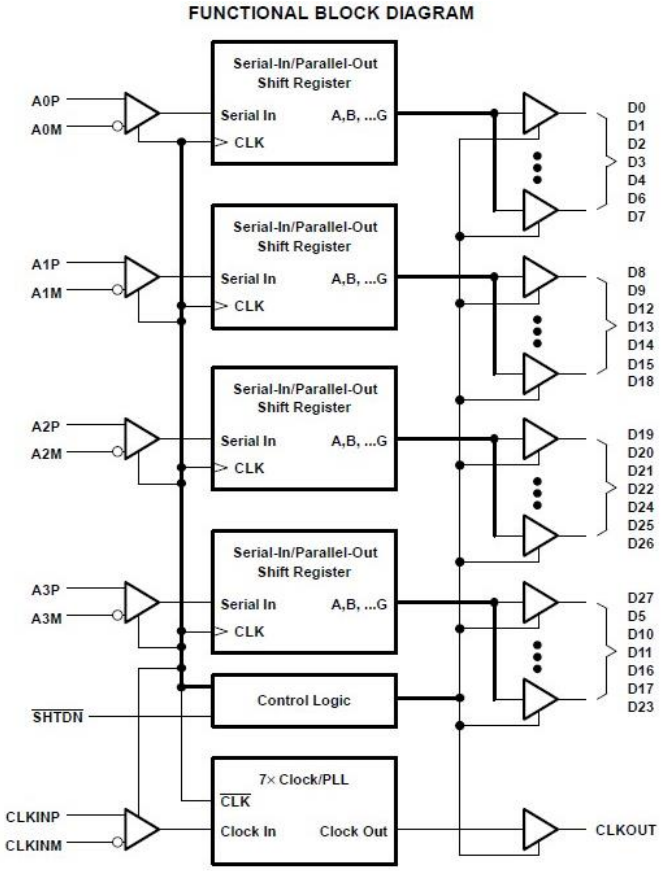
1. LVDS to RGB Functional Block



2. RECOMMENDED OPERATING CONDITIONS

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage ($\overline{SHTDN}$)	2			
V_{IL}	Low-level input voltage ($\overline{SHTDN}$)			0.8	
$\lvert V_{ID}\rvert$	Magnitude of differential input voltage	0.1		0.6	
V_{IC}, see Figure 2 and Figure 3	Common-mode input voltage	$\frac{\lvert V_{ID}\rvert}{2}$		$2.4 - \frac{\lvert V_{ID}\rvert}{2}$	
				V_{CC}-0.8	
T_A	Operating free-air temperature	-40		85	°C

TIMING REQUIREMENTS

		MIN	NOM	MAX	UNIT
t_c (1)	Input clock period	14.7	t_c	50	ns

(1) t_c is defined as the mean duration of a minimum of 32,000 clock periods.

PARAMETER MEASUREMENT INFORMATION

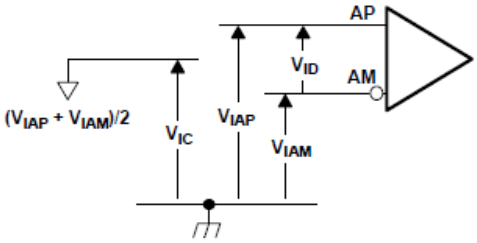


Figure 2. Voltage Definitions

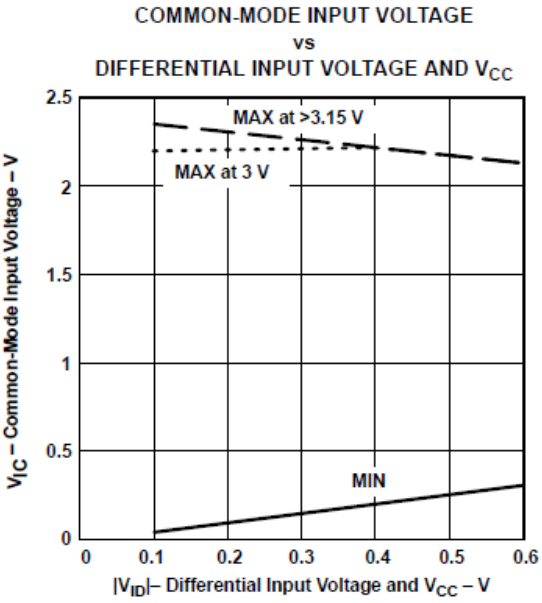
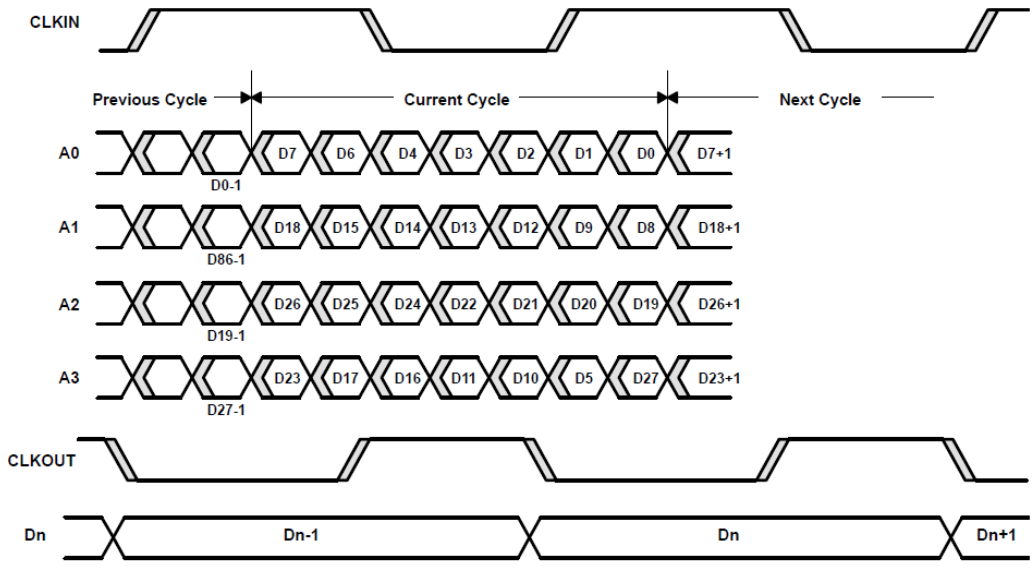


Figure 3. Recommended V_{IC} Versus V_{ID} and V_{CC}

3. Load and Shift Sequences



4. ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold				100	mV
V_{IT-}	Negative-going differential input voltage threshold(2)		-100			
V_{OH}	High-level output voltage	I_{OH} = -4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.4	V
I_{CC}	Quiescent current (average)	Disabled, all inputs open			280	µA
		Enabled, AnP at 1 V and AnM at 1.4 V, t_c = 15.38 ns		62	84	mA
		Enabled, C_L = 8 pF (5 places), Worst-case pattern, see Figure 4, t_c = 15.38 ns		107		mA
I_{IH}	High-level input current ($\overline{SHTDN}$)	$V_{IH} = V_{CC}$			±20	µA
I_{IL}	Low-level input current ($\overline{SHTDN}$)	V_{IL} = 0 V			±20	µA
I_{IN}	Input current (A and CLKIN inputs)	0 V ≤ V_I ≤ 2.4 V			±20	µA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}			±10	µA

(1) All typical values are V_{CC} = 3.3 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet for the negative-going input voltage threshold only.

5. SWITCHING CHARACTERISTICS

SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
t_{su}	Data setup time, D0 through D27 to CLKOUT	C_L = 8 pF	See Figure 5	4	6		ns
t_h	Data hold time, CLKOUT to D0 through D27			4	6		
t_{RSKM}	Receiver input skew margin(1), see Figure 6	t_c = 15.38 ns (±0.2%), |Input clock jitter| <50 ps(2)	T_A = 0°C to 85°C	490	800		ps
			T_A = -40°C to 0°C	390			
t_d	Delay time, input clock to output clock, see Figure 6	t_c = 15.38 ns (±0.2%)			3.7		ns
$\Delta t_{C(O)}$	Change in output clock period from cycle to cycle(3)	t_c = 15.38 + 0.75 sin (2π500E3t)±0.05 ns, See Figure 7			±80		ps
		t_c = 15.38 + 0.75 sin (2≠3E6t) ±0.05 ns, See Figure 7			±300		
t_{en}	Enable time, $\overline{SHTDN}$ to phase lock	See Figure 8			1		ms
t_{dis}	Disable time, $\overline{SHTDN}$ to Off state	See Figure 9			400		ns
t_t	Output transition time (t_r or t_f)	C_L = 8 pF			3		ns
t_w	Output clock pulse duration				0.43 t_c		ns

(1) t_{RSKM} is the timing margin available to allocate to the transmitter and interconnection skews and clock jitter. It is defined by $\frac{t_C}{14}$ –ts/h.
(2) |Input clock jitter| is the magnitude of the change in the input clock period.
(3) $\Delta t_{C(O)}$ is the change in the output clock period from one cycle to the next cycle observed over 15,000 cycles.

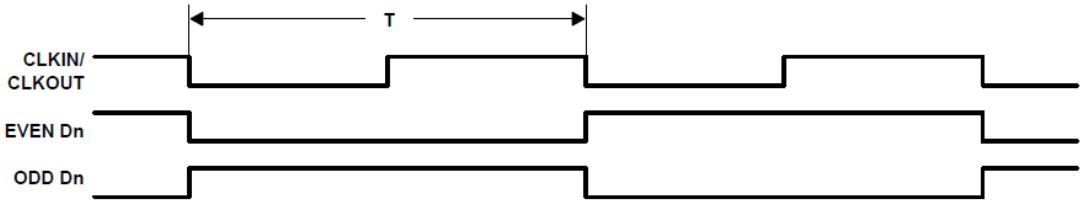


Figure 4. Worst-Case Power Test Pattern

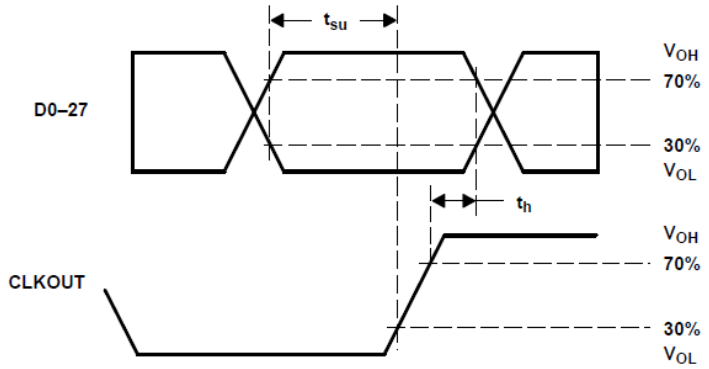


Figure 5. Setup and Hold Time Measurements

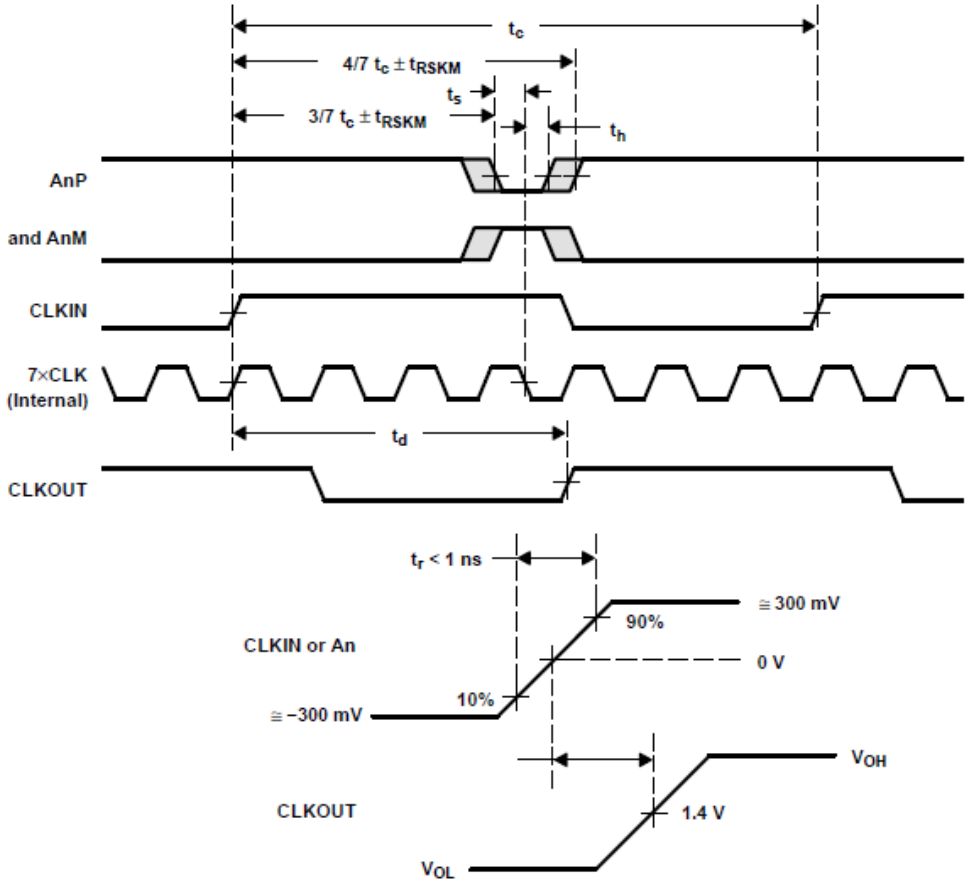


Figure 6. Receiver Input Skew Margin and t_d Definitions

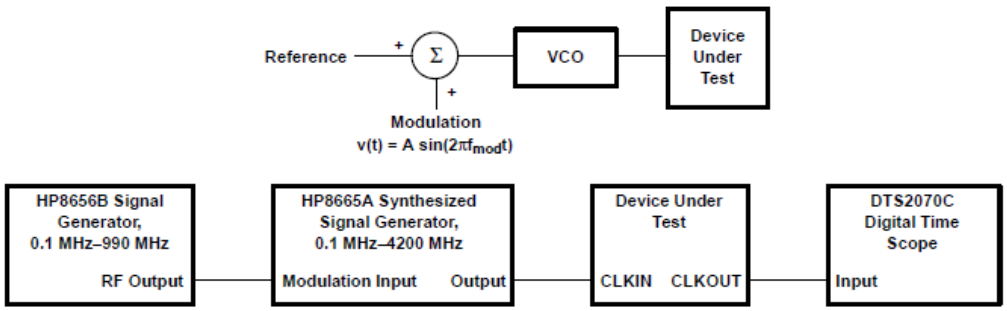


Figure 7. Output Clock Jitter Test Setup

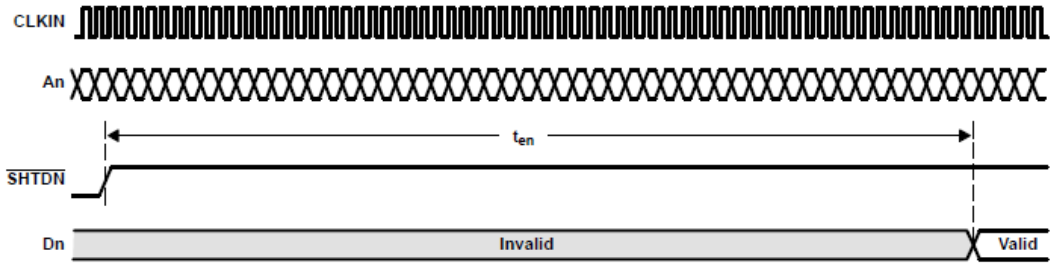


Figure 8. Enable Time Waveforms

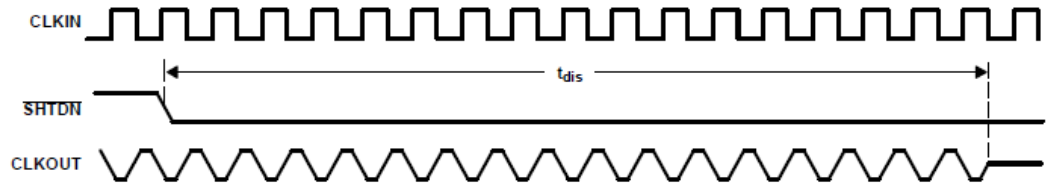


Figure 9. Disable Time Waveforms